

WHAT IS CLAIMED IS:

1. A verification apparatus comprising:
 - a circuit data unit including at least a processor;
 - a simulation device;
 - an expectation value generating device;
 - a comparing device;
 - an extracting device; and
 - an execution control device, wherein
the simulation device executes simulation of an
instruction executable by the processor in the circuit data
unit to thereby generate a simulation result,
the expectation value generating device generates an
expectation value when the instruction is executed,
the comparing device compares the simulation result to
the expectation value,
the extracting device extracts an information referenced
when the expectation value generating device generates the
expectation value or the generated expectation value, and
the execution control device judges whether or not the
instruction satisfies data restriction condition based on the
information extracted by the extracting device, and controls
the execution of the instruction in the simulation device and
the expectation value generating device based on a result of
the judgment.
- 25 2. The verification apparatus as claimed in Claim 1, wherein
the execution control device observes a value of a register
in which the information extracted by the extracting device
is stored to thereby judge whether or not the instruction
satisfies the data restriction condition.
- 30 3. The verification apparatus as claimed in Claim 1, wherein
the execution control device halts the execution of the
instruction in the simulation device and the expectation value
generating device based on the judgment result.

4. The verification apparatus as claimed in Claim 3, wherein
the extracting device extracts the instruction executed
in the expectation value generating device and a reference data
referenced when the instruction is executed, and

5 the execution control device comprises:
 a data restriction information storing unit for storing
presence or absence of restriction condition of the reference
data referenced when the instruction is executed and contents
of the restriction condition;

10 an instruction analyzing device for analyzing whether
or not the instruction has the data restriction condition by
collating the instruction and the reference data extracted by
the extracting device with the information stored in the data
restriction information storing unit;

15 a reference data analyzing device for analyzing whether
or not the reference data of the instruction satisfies the data
restriction condition by collating the instruction with the
information stored in the data restriction information storing
unit when the instruction has the data restriction condition;

20 and
 a control device for halting the simulation device and
the expectation value generating device when the reference data
of the instruction fails to satisfy the data restriction
condition.

25 5. The verification apparatus as claimed in Claim 1, wherein
 the simulation device comprises an execution standby
device for halting the simulation of the simulation device until
a halt release notice is received from the execution control
device,

30 the expectation value generating device comprises a prior
state shifting device for shifting a state of the expectation
value generating device back to a state before the last
instruction is executed, and

the execution control device comprises:

an undefined result judging device for judging whether or not the expectation value which is an execution result of the instruction in the expectation value generating device generates an undefined result which cannot be guaranteed as the execution result; and

5 a control device for making the execution standby device halt the execution of the instruction in the simulation device and making the prior state shifting device shift the state of
10 the expectation value generating device when a result of the judgment shows that the expectation value generates the undefined result.

6. The verification apparatus as claimed in Claim 1, wherein
15 the extracting device extracts the instruction executed in the expectation value generating device and a reference data referenced when the instruction is executed, and

the execution control device comprises:

a data restriction information storing unit for storing presence or absence of restriction condition of the reference
20 data referenced when the instruction is executed and contents of the restriction condition;

25 an instruction analyzing device for analyzing whether or not the instruction has the data restriction condition by collating the instruction and the reference data extracted by the extracting device with the information stored in the data restriction information storing unit;

30 a reference data analyzing device for analyzing whether or not the reference data of the instruction satisfies the data restriction condition by collating the instruction with the information stored in the data restriction information storing unit when the instruction has the data restriction condition; and

a control device for replacing the instruction with

another instruction not having the data restriction condition when the reference data of the instruction fails to satisfy the data restriction condition and executing the replaced another instruction in the simulation device and the expectation 5 value generating device.

7. The verification apparatus as claimed in Claim 1, wherein the extracting device extracts the instruction executed in the expectation value generating device and a reference data referenced when the instruction is executed, and 10 the execution control device comprises:

a data restriction information storing unit for storing presence or absence of restriction condition of the reference data referenced when the instruction is executed and contents of the restriction condition;

15 an instruction analyzing device for analyzing whether or not the instruction has the data restriction condition by collating the instruction and the reference data extracted by the extracting device with the information stored in the data restriction information storing unit;

20 a reference data analyzing device for analyzing whether or not the reference data of the instruction satisfies the data restriction condition by collating the instruction with the information stored in the data restriction information storing unit when the instruction has the data restriction condition;

25 and

a control device for correcting the instruction into another instruction whose reference data satisfies the data restriction condition when the reference data of the instruction fails to satisfy the data restriction condition and executing 30 the corrected instruction in the simulation device and the expectation value generating device.

8. The verification apparatus as claimed in Claim 7, wherein the control device replaces the reference data of the

instruction whose reference data fails to satisfy the data restriction conditions with another reference data satisfying the data restriction condition to thereby execute the replaced another instruction in the simulation device and the expectation
5 value generating device.

9. The verification apparatus as claimed in Claim 8, wherein the control device comprises:

10 a reference data candidate search device for searching another reference data candidate for the instruction whose reference data is judged not to satisfy the data restriction condition by the reference data analyzing device;

15 a reference data candidate analyzing device for analyzing whether or not the another reference data candidate searched by the reference data candidate search device satisfies the data restriction condition; and

a reference data replacing device for replacing the reference data with the another reference data candidate when the another reference data candidate satisfies the data restriction condition.

20 10. The verification apparatus as claimed in Claim 7, wherein the control device generates an update instruction for updating the reference data of the instruction referencing the reference data not satisfying the data restriction conditions, and executes the update instruction in the simulation device
25 and the expectation value generating device prior to the instruction timewise.

11. The verification apparatus as claimed in Claim 10, wherein the control device comprises:

30 an instruction generating device for generating the update instruction for updating the reference data of the instruction judged to reference the reference data not satisfying the data restriction condition by the reference data analyzing device into another reference data satisfying the

data restriction condition.

an instruction placing device for placing the update instruction so that the update instruction can be executed in the simulation device and the expectation value generating device prior to the instruction timewise.

5 12. The verification apparatus as claimed in Claim 1, wherein the extracting device extracts the instruction executed in the expectation value generating device and a reference data referenced when the instruction is executed, and

10 the execution control device comprises:

a data restriction information storing unit for storing presence or absence of restriction condition of the reference data referenced when the instruction is executed and contents of the restriction condition;

15 an instruction analyzing device for analyzing whether or not the instruction has the data restriction condition by collating the instruction and the reference data extracted by the extracting device with the information stored in the data restriction information storing unit;

20 a reference data analyzing device for analyzing whether or not the reference data of the instruction satisfies the data restriction condition when the instruction has the data restriction condition; and

25 a control device for forcibly updating the reference data of the instruction so as to satisfy the data restriction condition in the simulation device and the expectation value generating device when the reference data of the instruction fails to satisfy the data restriction condition.

30 13. The verification apparatus as claimed in Claim 1, wherein the extracting device extracts the instruction executed in the expectation value generating device and a reference data referenced when the instruction is executed, and

 the execution control device comprises:

a data restriction information storing unit for storing presence or absence of restriction condition of the reference data referenced when the instruction is executed and contents of the restriction condition;

5 an instruction analyzing device for analyzing whether or not the instruction has the data restriction condition by collating the instruction and the reference data extracted by the extracting device with the information stored in the data restriction information storing unit;

10 a reference data analyzing device for analyzing whether or not the reference data of the instruction satisfies the data restriction condition when the instruction has the data restriction condition; and

15 a control device for updating the simulation result and the expectation value which are obtained as a result of the execution of the instruction in the simulation device and the expectation value generating device so that the simulation result and the expectation value have an equal value when the reference data of the instruction fails to satisfy the data restriction condition.

20

14. The verification apparatus as claimed in Claim 1, wherein the extracting device extracts the instruction executed in the expectation value generating device and a reference data referenced when the instruction is executed, and

25 the execution control device comprises:

26 a data restriction information storing unit for storing presence or absence of restriction condition of the reference data referenced when the instruction is executed and contents of the restriction condition;

30 an instruction analyzing device for analyzing whether or not the instruction has the data restriction condition by collating the instruction and the reference data extracted by the extracting device with the information stored in the data

restriction information storing unit;

a reference data analyzing device for analyzing whether or not the reference data of the instruction satisfies the data restriction condition when the instruction has the data 5 restriction condition; and

a control device for generating an update instruction for updating the simulation result and the expectation value which are obtained as a result of the execution of the instruction in the simulation device and the expectation value generating device and executing the update instruction in the simulation 10 device and the expectation value generating device when the reference data of the instruction fails to satisfy the data restriction condition.

15. A verification method in which a simulation result of an instruction is obtained through simulation of the instruction in a circuit data unit including at least a processor and an expectation value when the instruction is simulated is obtained by means of the instruction so that the circuit data unit is verified based on comparison of the simulation result and the 20 expectation value, comprising:

an extracting step for extracting an information referenced when the expectation value is generated or the generated expectation value;

a judging step for judging whether or not the instruction satisfies data restriction condition based on the information extracted in the extracting step; and

a control step for controlling the simulation of the instruction and the generation of the expectation value of the instruction based on a result of the judgment in the judging 30 step.

16. The verification method as claimed in Claim 15, wherein a value of a register in which the information extracted in the extracting step is stored is observed so that it is judged

whether or not the instruction satisfies the data restriction conditions in the control step.

17. The verification method as claimed in Claim 15, wherein the data restriction conditions include conditions which
5 restrict a value range of the reference data.

18. The verification method as claimed in Claim 15, wherein the simulation of the instruction and the generation of the expectation value of the instruction are halted based on the judgment result of the judging step in the control step.

10 19. The verification method as claimed in Claim 18, wherein the extracting step includes a step of extracting the instruction for generating the expectation value and the reference data referenced when the expectation value of the instruction is generated, and

15 the control step comprises:

an instruction analyzing step for analyzing whether or not the reference data of the instruction extracted in the extracting step has data restriction condition;

20 a reference data analyzing step for analyzing whether or not the reference data of the instruction satisfies the data restriction conditions when the instruction has the data restriction condition; and

25 a control step for halting the simulation of the instruction and the generation of the expectation value of the instruction when the reference data of the instruction fails to satisfy the data restriction condition.

20. The verification method as claimed in Claim 19, wherein the simulation of the instruction and the generation of the expectation value of the instruction are halted until the
30 instruction not having the data restriction condition or the instruction satisfying the data restriction condition is supplied as a next instruction in the control step.

21. The verification method as claimed in Claim 15, wherein

the simulation of a next instruction and the generation of the expectation value of the next instruction executed subsequent to the instruction are controlled based on the judgment result of the judging step in the control step.

5 22. The verification method as claimed in Claim 21, wherein the simulation of the instruction is halted, and the generation of the expectation value of the instruction is shifted back to a state prior to the generation based on the judgment result of the judging step in the control step.

10 23. The verification method as claimed in Claim 22, wherein the expectation value obtained through the generation of the expectation value of the instruction is extracted in the extracting step, and

the control step comprises:

15 an undefined result judging step for judging whether or not the expectation value obtained through the generation of the expectation value of the instruction generates an undefined result which cannot be guaranteed as an execution result of the instruction; and

20 a prior state shifting step for halting the simulation of the instruction and shifting the generation of the expectation value of the instruction back to the state prior the generation when a result of the judgment shows that the expectation value generates the undefined result.

25 24. The verification method as claimed in Claim 15, wherein the extracting step includes a step of extracting an instruction executed in the expectation value generation and a reference data referenced when the instruction is executed, and

30 the control step comprises:

an instruction analyzing step for analyzing whether or not the instruction has the data restriction condition by collating the instruction and the reference data extracted in

the extracting step with restriction conditions of the reference data referenced when the instruction is executed;

5 a reference data analyzing step for analyzing whether or not the reference data of the instruction satisfies the data restriction condition by collating the reference data of the instruction with the restriction conditions of the reference data referenced when the instruction is executed when the instruction has the data restriction condition; and

10 a control step for replacing the instruction with another instruction not having the data restriction conditions when the reference data of the instruction fails to satisfy the data restriction conditions, simulating the replaced another instruction and generating the expectation value of the replaced another instruction.

15 25. The verification method as claimed in Claim 15, wherein the extracting step includes a step of extracting an instruction executed in the generation of the expectation value and a reference data referenced when the instruction is executed, and

20 the control step comprises:

an instruction analyzing step for analyzing whether or not the instruction has the data restriction condition by collating the instruction and the reference data extracted in the extracting step with restriction conditions of the reference data referenced when the instruction is executed;

25 a reference data analyzing step for analyzing whether or not the reference data of the instruction satisfies the data restriction condition when the instruction has the data restriction condition; and

30 a control step for correcting the instruction into another instruction whose reference data satisfies the data restriction condition, simulating the corrected instruction and generating the expectation value of the corrected instruction when the

reference data of the instruction fails to satisfy the data restriction condition.

26. The verification method as claimed in Claim 25, wherein
the reference data of the instruction is replaced with
5 another reference data satisfying the data restriction condition when the reference data of the instruction fails to satisfy the data restriction condition in the control step.

27. The verification method as claimed in Claim 26, wherein
the control step comprises:

10 a candidate search processing for searching another reference data candidate for the instruction analyzed to have the reference data not satisfying the data restriction condition in the reference data analyzing step;

15 a candidate analyzing processing for analyzing whether or not the another reference data candidate searched in the candidate search processing satisfies the data restriction condition; and

20 a reference data replacing processing for replacing the reference data with the another reference data candidate satisfying the data restriction condition.

28. The verification method as claimed in Claim 25, wherein
an update instruction for updating the reference data of the instruction into another reference data satisfying the data restriction condition is generated when the reference data 25 of the instruction fails to satisfy the data restriction condition, the reference data is updated based on the update instruction, and the instruction is simulated and the expectation value of the instruction is generated in the control step.

30 29. The verification method as claimed in Claim 28, wherein
the control step comprises:

an update instruction generating processing for generating the update instruction for updating the reference

data of the instruction into the another reference data satisfying the data restriction conditions when the reference data of the instruction fails to satisfy the data restriction conditions; and

5 an instruction placing processing for placing the update instruction so that the update instruction is executed before the simulation of the instruction and the generation of the expectation value of the instruction.

30. The verification method as claimed in Claim 15, wherein
10 the reference data is updated into data satisfying the data restriction conditions when it is judged in the judging step that the reference data fails to satisfy the data restriction conditions in the control step.

31. The verification method as claimed in Claim 30, wherein
15 the extracting step includes a step of extracting an instruction executed in the generation of the expectation value and a reference data referenced when the instruction is executed, and

 the control step comprises:

20 an instruction analyzing step for analyzing whether or not the instruction has the data restriction condition by collating the instruction and the reference data extracted in the extracting step with restriction conditions of the reference data referenced when the instruction is executed;

25 a reference data analyzing step for analyzing whether or not the reference data of the instruction satisfies the data restriction condition when the instruction has the data restriction condition; and

30 a control step for forcibly updating the reference data into another reference data satisfying the data restriction condition, simulating the instruction and generating the expectation value of the instruction when the reference data of the instruction fails to satisfy the data restriction

condition.

32. The verification method as claimed in Claim 24, wherein
the simulation result and the expectation value obtained
through the simulation of the instruction and the generation
of the expectation value of the instruction are updated to have
an equal value when it is judged in the judging step that the
reference data fails to satisfy the data restriction conditions
in the control step.

33. The verification method as claimed in Claim 32, wherein
the extracting step includes a step of extracting an
instruction executed in the generation of the expectation value
and a reference data referenced when the instruction is executed,
and

the control step comprises:

15 an instruction analyzing step for analyzing whether or
not the instruction has the data restriction condition by
collating the instruction and the reference data extracted in
the extracting step with restriction conditions of the reference
data referenced when the instruction is executed;

20 a reference data analyzing step for analyzing whether
or not the reference data of the instruction satisfies the data
restriction condition when the instruction has the data
restriction condition; and

25 a control step for updating the simulation result and
the expectation value obtained through the simulation of the
instruction and the generation of the expectation value of the
instruction so as to have an equal value when the reference
data of the instruction fails to satisfy the data restriction
condition.

30 34. The verification method as claimed in Claim 32, wherein
the simulation result is updated to have a value equal
to the expectation value, or the expectation value is updated
to have a value equal to the simulation result in the control

step.

35. The verification method as claimed in Claim 15, wherein
the extracting step includes a step of extracting an
instruction executed in the generation of the expectation value
5 and a reference data referenced when the instruction is executed,
and

the control step comprises:

an instruction analyzing step for analyzing whether or
not the instruction has the data restriction condition by
10 collating the instruction and the reference data extracted in
the extracting step with restriction conditions of the reference
data referenced when the instruction is executed;

15 a reference data analyzing step for analyzing whether
or not the reference data of the instruction satisfies the data
restriction condition when the instruction has the data
restriction condition; and

20 a control step for generating an update instruction for
updating the simulation result and the expectation value
obtained through the simulation of the instruction and the
generation of the expectation value of the instruction and
executing the update instruction after the simulation of the
instruction and the generation of the expectation value of the
instruction when the reference data of the instruction fails
to satisfy the data restriction condition.